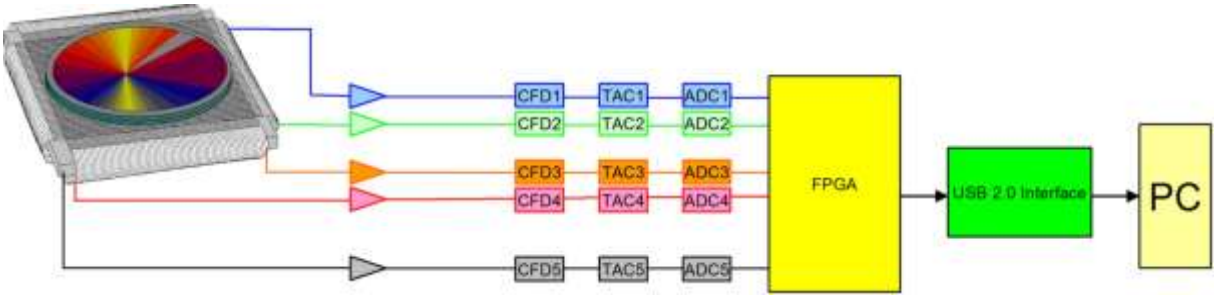
Roadmap to the development of a 1,04 GHz - 4 (x v4) - segment delay line detector providing a time resolution of ~50 ps

Surface Concept is well on its way to developing a fast delay line detector system capable of a count rate acquisition of 1.04 GHz. Development is divided into three major steps. The operation principle of the current detector system will be maintained; position information is obtained by time difference measurements, while each event can be assigned to an absolute time. The time base is correlated to an external reference signal. The precision of time reference measurements will be 50 ps or below, while the time difference measurements will achieve an accuracy of about 25 ps. In two intermediate steps we will design a miniaturized detector version that is manufactured by photo-lithographic methods to work at 15 MHz count rates for the first and 260 MHz for the second development step, reaching a time resolution of 80 ps or below. The outcome of the second step will be optimized in phase 3; the time resolution will be improved to 50 ps or below and further a high count rate fourfold detector will be built consisting of four independent detector/readout units. This four segment solution is intended to be able to detect events with a count rate of up to 1.04 GHz distributed over the active area. These events will be sorted by position and time into a large histogram based memory unit that can be transferred to a PC. Further cascading can be done without large efforts.

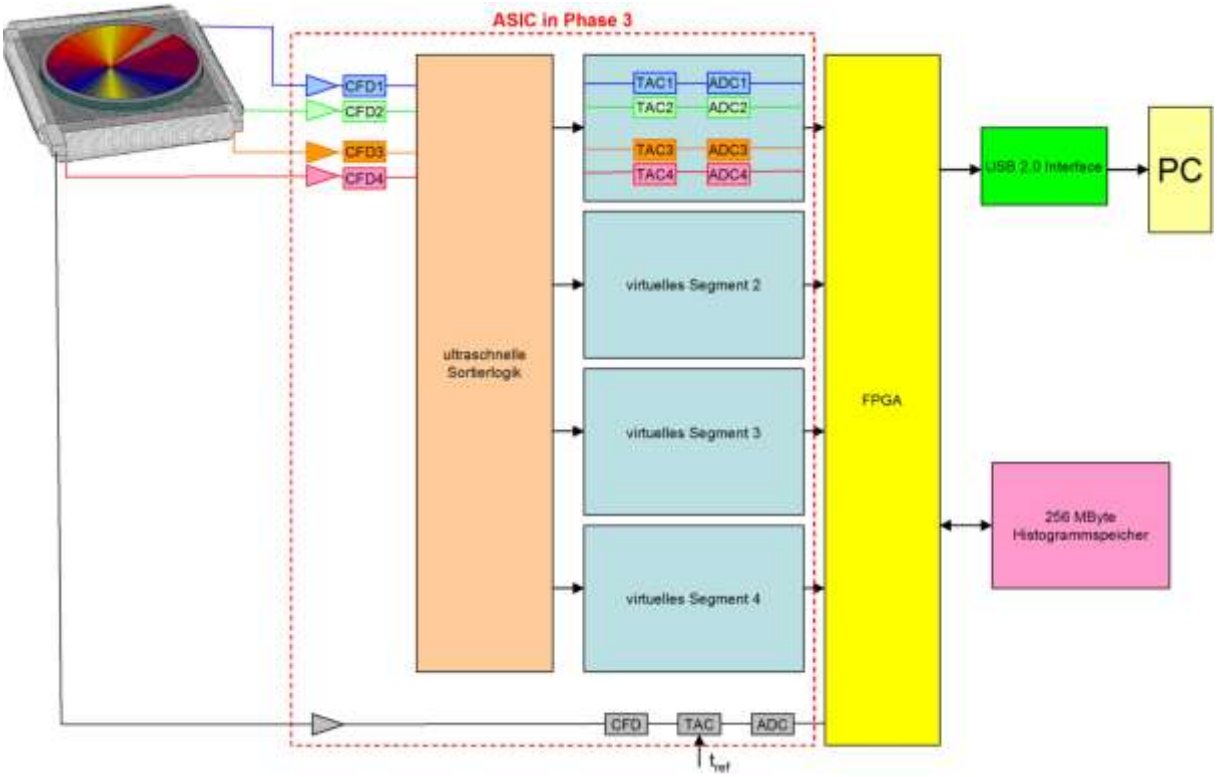
Step 1: 15 MHz:

A non-segmented delayline detector with a typical loop transfer time of about 400 ps enables position encoding at 1000 x 1000 pixels at an active area of 20 mm x 20 mm. The time coordinate will be resolved using 12 bit dynamics (4096 channels at 80 ps resolution each). The maximum travel time of pulses at the delay wires will be limited to about 40 ns. The read-out unit consists of 5 analogue time measurement modules followed by 65 MHz ADCs which are coupled to an FPGA. This unit may be linked to a computer using a USB 2.0 interface like in our solution that was completed in spring 2004. One of the read-out channels is used for time reference measurements, the other 4 provide the position determination. All 5 measurements are needed to determine each event, so the electronics limits this solution to 65MHz count rate. On the other hand the maximum travel time along the delay lines would not enable this count rate. Therefore, the USB 2.0 interface is still sufficient (480 Mbit/s) for direct data transfer. The maximum transferable count rate will be limited to 15 MHz, because each event is transferred to the computer with a size of 4 bytes.



Step 2: 260 MHz:

The photolithographically manufactured detector of step 1 will be redesigned to use loop transfer times of 205 ps, while the read-out distinguishes between the left and right half of both delaylines. The unit will be implemented 4 times building up a virtual 4 fold segmentation. An event time sorting logic supplies the 4 read out lines with pulses originating from the 4 quadrants of the physically unsegmented detector. Thus, the electronics consists of 17 channels each equipped with a 65 MHz ADC (4 x 4 ch for position, 1 ch for time encoding). The event assignment to the four virtual segments will be done by means of an ultra-fast logic unit already being under development by Surface Concept. The faster loop transfer time enables maximum travel times along the delay lines of 20 ns, i.e. 10 ns per each delayline half. Therefore all quadrants may be read out with a maximum of 65 MHz. Thus, this concept enables count rates up to 260 MHz with a position encoding by 512 x 512 pixels at an active area of 20 mm x 20 mm. Again, the 17 channel unit is coupled to an FPGA, but no direct data transfer to the PC will be realized. The FPGA sorts all results into a 256 MByte histogram memory, organized as x,y,t such as a 3 dimensional array of - for example - 9 bits x 9 bits x 9 bits having a 2 byte dynamics (memory unit depth). The number of time channels might be reorganized to higher resolution at cost of the number of position channels. The USB 2.0 interface still handles the block transfers from the histogram memory into the PC.



Step 3: 1.04 GHz:

The multi-channel scheme of step 2 will be integrated in an ASIC design mainly to enable cascading of this solution. At the same time, the time resolution for position encoding will be improved to about 25 ps.

Adaption of pulse width and propagation dispersion is needed for matching of MCPs and electronics to reach the 25 ps resolution. 350 ps pulse widths at 2 µm pore size are considered to use (www.photonis.com). The analogue amplifiers will be exchanged by modules working at bandwidths in the GHz region. The design of the detector itself has to be adapted to the needs of small pulse widths and loop dispersion as well as wire distances must match high count rates resulting in pulse handlings at ≤2 ns overall FWHM without changes in the functional principle of the delayline detector. A thick film technique will be applied to produce a 4 fold delayline detector working at these optimized parameters. The active area of all 4 detector segments might be scaled to reach a maximum of 40 mm x 40 mm. Smallest active areas are expected to be about 10 mm x 10 mm resulting in a position resolution of about 10 µm. The total number of pixels for this solution may be 1024 x 1024. Further cascaded designs of more segments are possible to produce in the same way. The 260 MHz read-out unit will be used four times (max. 1.04 GHz). An additional processor will control the data transfer from all four 256 MByte histogram memory blocks into the PC using a transfer interface that still has to be determined.

Notes concerning data acquisition:

The measured results of the four 260 MHz segments are stored in separated histogram memories organized in 3D (x,y,t). It makes sense to define a flexible organization of the memories, such as (8 bit x 8 bit x 10 bit), (7 bit x 7 bit x 12 bit), (6 bit x 6 bit x 14 bit), or (5 bit x 5 bit x 16 bit) at 4 Byte memory unit depth and to include the option of a selectable binning of the time channels. Thus, the option providing maximum position resolution enables 1024 x 1024 pixels with 4 Byte pixel dynamics for very long acquisition times into the histogram memory at a count rate of 1 GHz.

Our partners for this development:

In the framework of this roadmap we are working together with specialized and well established partners. This network bundles expertise and special knowledge at different fields that are of outstanding interest for the development of a 1.04 GHz delayline detector with a time resolution of ~50 ps.

SPECS

RoentDek Handels GmbH
Supersonic Gas Jets
Detection Techniques
Data Acquisition Systems
Multifragment Imaging Systems

gammadata

point electronic

hms media solutions

PREMA SEMICONDUCTOR

LaVision BioTec

N-HANDS THE EMBEDDED COMPOSERS

Published solutions and other opportunities

This roadmap is mainly focused on improvements of the read-out system of our detectors by parallel designs. Other pico-second measurement devices on the market could be taken into account. Nevertheless it would need a comparable effort to adapt such systems to the needs of our roadmap like the sketched development does. It might be interesting to adapt the concept if further improvements could be expected. Currently, the time measurements are done by means of TDCs, which are often restricted to maximum count rate transfers to a couple of MHz. For instance, the company Hypres Inc. / Elmsford, USA has developed a 2 ps TDC which might be able to transfer count rates up to 30 GHz in the framework of a funded project (DOE Grant No. DE-FG02-98ER82595). If this work succeeds and such instruments would be available commercially, then the 1 GHz limit seems not to be the termination of this development.