Imaging Particle Detectors, Electron Optics, Ultrafast Dynamics, Delay Line Detectors, Piscosecond Detection Systems, Electronics

SURFACE CONCEPT

Time-to-Digital-Converters (TDCs)

The Surface Concept Time-to Digital-Converters (TDCs) are compact, fast and user-friendly devices that are available with a variety of performance characteristics. Possible layouts include stand-alone housings and NIM modules (2/12). All TDCs are equipped with a high-speed USB 2.0 interface.

Layout of the SC-TDC-1000/08 S combining 1 start / 8 stop channels with a time resolution of 82.2ps* (individual improvements down to 64 ps).

Basic device features

- LVTTL or NIM (PECL optional) inputs, common start input usable as reset of the internal clock
- Internal clock quartz-accurate, resolution adjust PLL, i.e. insensitive to temperature / voltage variations, adjustable via software (no calibration necessary)
- 8 or 16 stop channels, 1 start channel at a resolution of 82 ps*, measurement range 0 ns – 10.7 µs in start-stop operation
- 2 or 4 stop channels, 1 start channel at a resolution of 27 ps*, measurement range 0 ns – 40 µs in start-stop operation
- Min. time between start and stop 0 ns, pulse pair resolution 5.5 ns, min. 32 hits / ch. multihit capability
- No minimum time limit for hits at different channels
- Measurement rate up to 8 million results per second via USB 2.0 (up to 80 million results per second optional, using FPGA features, see options)

Customized TDC type 03-06-27 (3 start / 6 stop channels with a time resolution of 27.4ps) housed in a 2/12 unit NIM-module.

A variety of optional extensions is available (see next page)

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*Values for time resolution can be improved by software adjustments down to typically 85 % of the here given bin size values, e.g. R-Mode: typ. value 27.4 ps, best value 21 ps.

Options (as single or combined options available)

1. **Sync IN / OUT option:** Additional input and output (BNC-type connector, LVTTL) for synchronization of TDC with external devices.

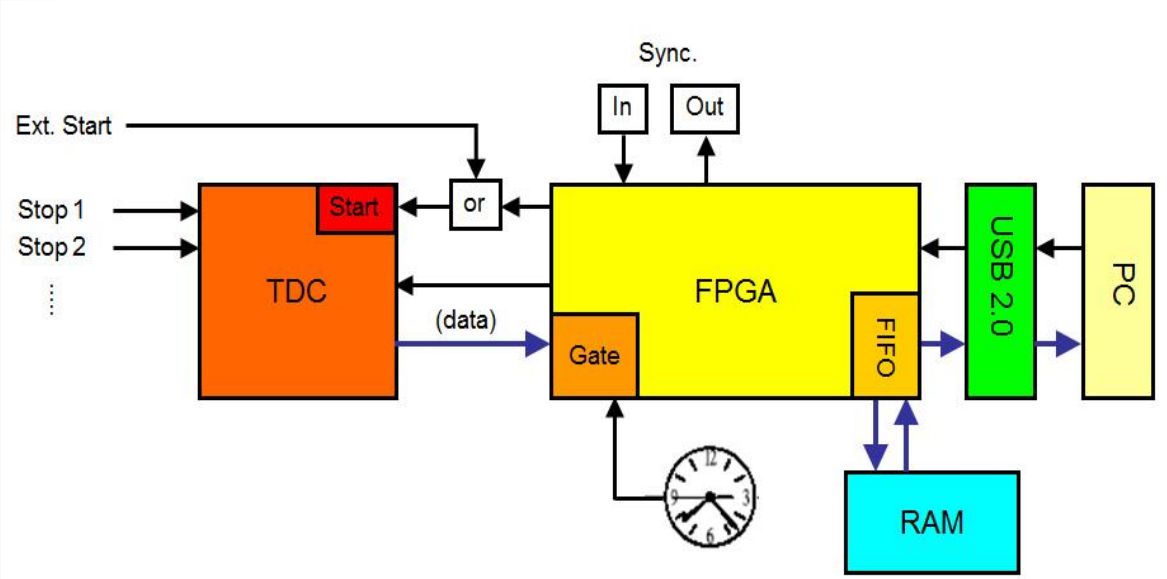
2. **Extended measurement range option:** Extension of the measurement range by transfer and evaluation of a start counter and use of a stop channel as time reference, respectively (14.7ms for devices with 27.4ps time resolution, and 44.2ms for devices with 82.2ps time resolution).

3. **Start divider option:** Internal programmable frequency divider of the start input.

4. **Level converter option:** Internal conversion of the input signal levels from any established type.

5. **Linux option:** Linux drivers and software provided.

6. **PLU-option:** FPGA pre-conditioning feature, enables extended functionality, e.g.: (to a certain extent user specific features are possible)
    - 80 MHz data acquisition rate using the FPGA pre-conditioning of hardware histogramming
    - Additional I/O lines for streaming of logical states or with counters
    - Quartz stabilized, free programmable, global time gate (100 ns – 24 h)



Operation principle of the Surface Concept USB 2.0 TDC. Extended functionality can be realized by programming the FPGA as described in the section „PLU-option“.

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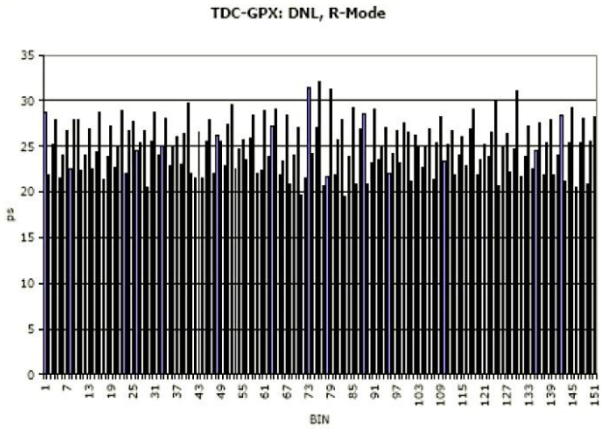
Technical data of basic operation modes

I-Mode

- 8 channels with 82.2ps* BIN (INL 1 LSB)
- 5.5ns pulse-pair resolution with 32-fold multi-hit capability = 185MHz peak rate
- Trigger on rising or falling edge
- Measurement range 0ns – 10.7µs

R-Mode

- 2 channels with 27.4ps* BIN (INL 1.4 LSB)
- 5.5ns pulse-pair resolution with 32-fold multi-hit capability = 185MHz peak rate
- Trigger on rising or falling edge
  Measurement range 0ns up to > 40µs



Typ. DNL (differential non-linearity) for R-Mode

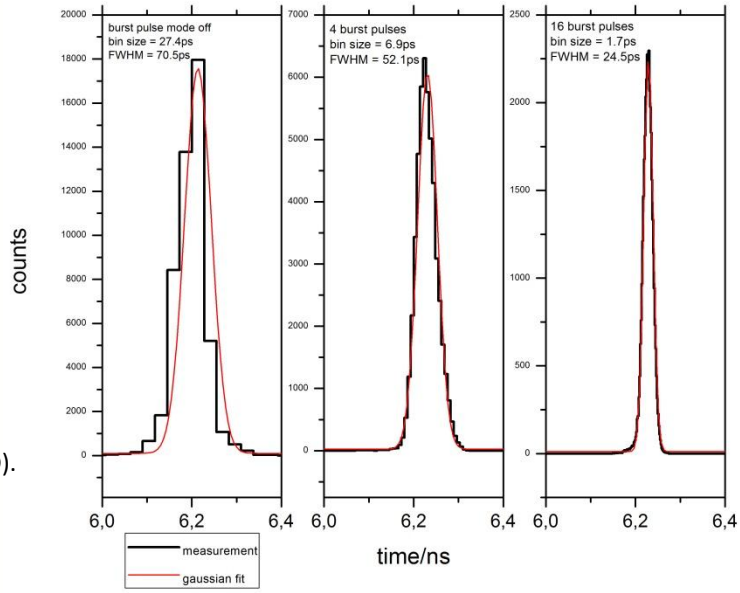
Highest time resolution

In combination with the measurement time extension layout, another device option is available for the high resolution models (SC-TDC-1000/02 D and SC-TDC-1000/04 D, see next page):

Burst Option

In order to increase the time resolution each event is multiplied internally by means of hardware and is measured multiple times. Theoretically, the time resolution of such a measurement is improved by a factor of SQRT(N) where N is the number of multiple time measurements of the same event. The burst mode can be used in combination with all modes described earlier with the restriction of an appropriately extended dead time (Burst Pulse Option will restrict the min. pulse pair time distance of the device to about 8ns).

Improvement of time resolution in burst operation (measured with SC-TDC.1000/04 D).



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Available Layouts

Stand-alone TDCs

SC-TDC-1000/02 D

- 1 GPX chipset
- 2 stops, 1 start (NIM, diff. LVPECL optional)
- 2 BNC I/O control terminals for synchronisation optional
- 27.4* / 41.1ps* time bin in R / G – Mode
- 40 MHz internal readout rate, data transfer rate up to 35 Mbyte / s
- DLL compatible with Windows XP®, Windows Vista® and Windows 7® 32 bit operating systems (Linux optional)
- LabVIEW™ interface available

SC-TDC-1000/04 D

- 2 GPX chipsets
- 4 stops, 1 start (NIM, diff. LVPECL optional)
- 2 BNC I/O control terminals for synchronization optional
- 27.4* / 41.1ps* time bin in R / G – Mode
- 80 MHz internal readout rate, data transfer rate up to 35 Mbyte / s
- DLL compatible with Windows XP®, Windows Vista® and Windows 7® 32 bit operating systems (Linux optional)
- LabVIEW™ interface available

SC-TDC-1000/08 S

- 1 GPX chipset
- 8 stops (LVTTL), 1 start (LVTTL)
- 2 BNC I/O control terminals for synchronization optional
- 82.2ps* time bin in I – Mode
- 40 MHz internal readout rate, data transfer rate up to 35 Mbyte / s
- DLL compatible with Windows XP®, Windows Vista® and Windows 7® 32 bit operating systems (Linux optional)
- LabVIEW™ interface available

SC-TDC-1000/16 S

- 2 GPX chipset
- 16 stops (LVTTL), 1 start (LVTTL)
- 2 BNC I/O control terminals for synchronization optional
- 82.2ps* time bin in I – Mode
- 80 MHz internal readout rate, data transfer rate up to 35 Mbyte / s
- DLL compatible with Windows XP®, Windows Vista® and Windows 7® 32 bit operating systems (Linux optional)
- LabVIEW™ interface available

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SC-TDC-1000/16 D fourfold quad-channel USB 2.0 TDC

The fourfold quad-channel USB 2.0 TDC consists of 4 independently working TDC / FPGA units. Optionally, a programmable logic unit (PLU) enables comfortable data preconditioning and a variable data stream handling via USB 2.0.

Customer specific layout of the fourfold quad-channel USB 2.0 TDC operating in R-Mode with 16 stop channels on 4 HDMI connectors.

Basic device features

- 64 stop channels at a digital time bin size of 82.2ps*, measurement range 0 ns – 10.7µs in start-stop operation (infinite measurement range by internal retriggering available, optional)
- 16 stop channels at a digital time bin size of 27.4ps*, measurement range 0 ns – 40µs in start-stop operation
- Higher number of stop channels on request (e.g. 128 stop channel version)
- Event memory space for up to 30 million events (4 x 32 Mbyte memory)
- Equivalent count rates of > 1 billion bytes per second into internal memory space (for short bursts only)
- Programmable logic unit (PLU) available on request for a comfortable data preconditioning and a variable data stream handling via USB 2.0

The fourfold quad-channel USB 2.0 TDC is available in 2 different operation modes:

I-Mode

- Time bin resolution of 82.2ps* per channel ($\sigma \cong 1$ bin)
- 64 stop channels referring to 1 start channel (8 groups of 8 stop channels possible, using 8 separated start inputs)
- Measurement range 0 ns – 10.7µs (10.7µs corresponds to a restart frequency of 93.5kHz)
- 5.5ns pulse-pair resolution with 32-fold multi-hit capability for each channel, 0ns
- between channels
- Start-retrigger frequency max. 7MHz
- Trigger to rising or falling edge

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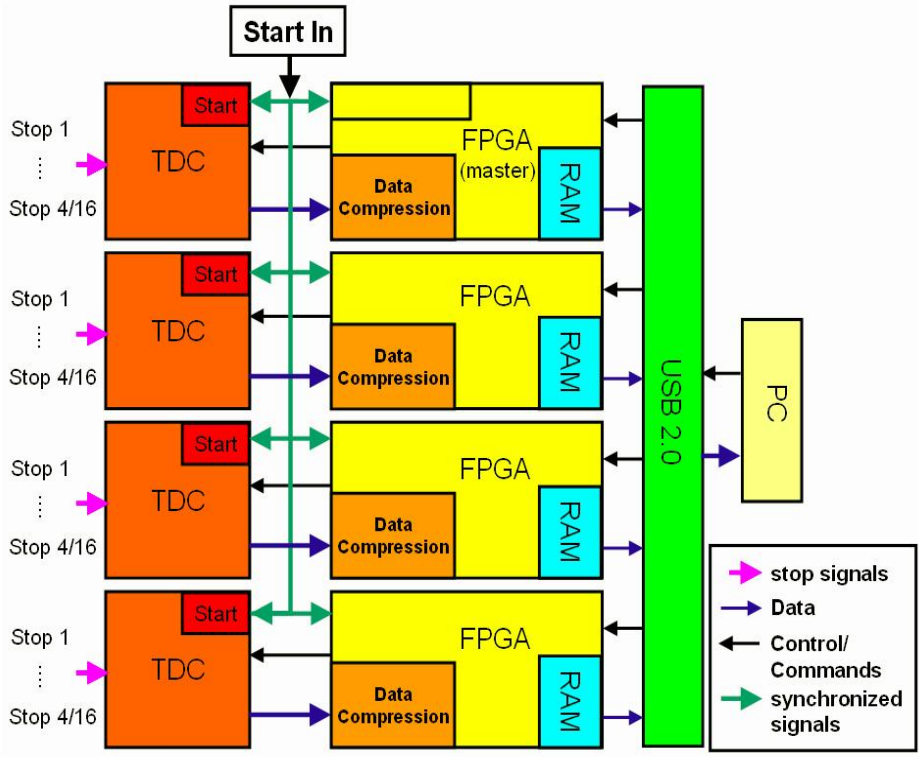
R-Mode

- Time bin resolution of 27.4ps* per channel ($\sigma \cong 1.4$ bins for short measurement range)
- 16 stop channels referring to 1 start channel (8 groups of 2 stop channels possible, using 8 separated start inputs)
- Measurement range 0ns – 40µs (40µs corresponds to a restart frequency of 25kHz)
- 5.5ns pulse-pair resolution with 32-fold multi-hit capability for each channel, 0ns
- between channels
- Start-retrigger frequency max. 9MHz
- Trigger to rising or falling edge



Schematic layout of fourfold quad channels USB 2.0 TDC with FPGA assisted data compression.

Count rate limitations

Limitation by writing into internal memory

The maximum possible count rate which can be reached is limited by the writing speed into the internal memory. The fourfold quad channel USB 2.0 TDC consists of 4 independent TDC units. Each TDC unit fullfills the following specifications:

- Maximum writing speed into memory: 73.6 million counts per second distributable over 16 / 4 stop channels in I / R mode
- Maximum writing speed per single stop channel: 9.2 million counts per second / 36.8 million counts per second in I / R mode.

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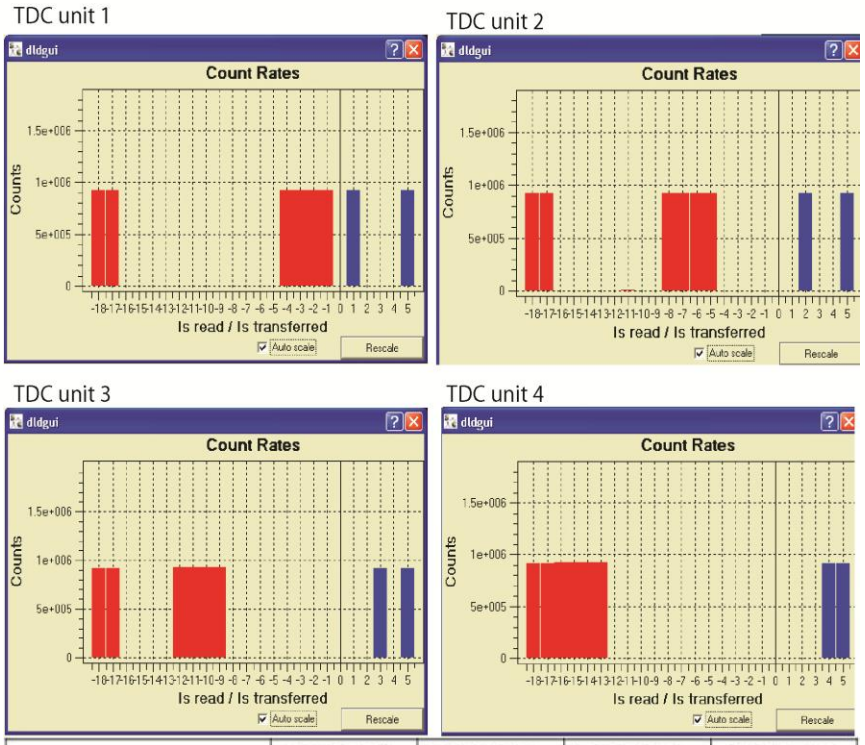
Thus, the entire fourfold quad channel USB 2.0 TDC with 4 TDC units enables the transfer of 295.0 million results of full 32 bit dynamics per second (1.18 billion results per second for 8 bit dynamics) into the internal memory space. Typical test results at the transfer limit with 32 bit dynamics (using a burst length of 50 ms) are shown in the following figure.



	TDC Unit 1	TDC Unit 2	TDC Unit 3	TDC Unit 4
Counts per stop channel within 50 ms short burst	923.067 (coincident in all 4 channels)	921.862 (coincident in all 4 channels)	921.960 (coincident in all 4 channels)	920.214 (coincident in all 4 channels)
Equivalent coincidence rate per 4 stop channel in counts per second	18.461.340	18.437.240	18.439.200	18.404.280
Equivalent count rate per single stop channel in counts per second	73.845.360	73.748.960	73.756.800	73.617.120

For these test measurements each of the 4 TDC units was searching for fourfold stop coincidences on all of its 4 stop channels. Burst rate limit measurements of all 16 stop channels of a fourfold quad channel USB 2.0 TDC operated in R-Mode. TDC readout was performed with the Surface Concept GUI monitor software. Bars at -17 / -18 represent the identified coincidences. Blue bars represent the number of coincidence results that have been transferred via USB 2.0 to the PC.

Limitation by data transfer via USB 2.0

The maximum count rate for a permanent event streaming into the PC via USB 2.0 is limited to 35 million bytes per second. This limit corresponds to a transfer rate of 8.75 million time results with full measurement dynamics, if data are send in raw data format without any FPGA-assisted data compression. Depending on the user application, data dynamics may be reduced or an appropriate data compression could increase the rate of the streamed data.

NIM TDCs (2/12)

- NIM, LVPECL (low voltage PECL) or LVTTL (low voltage TTL) inputs
- 8 stop channels at a time bin resolution of 82.2ps* time resolution, measurement range 0 ns – 10.7µs in start-stop operation (double TDC option: 16 stop channels, 1 or 2 start channels)
- 2 stop channels at a time bin resolution of 27.4ps* time resolution, measurement range 0 ns – 40µs in start-stop operation (double TDC option: 4 stop channels, common start input)
- measurement range extendable on request
- Min. time between start and stop 0 ns, pulse pair resolution 5.5ns, min. 32 hits / channel
- Multi-hit capability extendable by FPGA options (e.g. hit tagging, see options)
- No miminum time limit for hits at different channels
- Transfer rate up to 8 million results per second via USB 2.0 readout (interface available for Windows XP®, Windows Vista® and Windows 7® 32 bit operating systems)
- LabVIEW™ interface available
- DLL for user programming

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